Carnegie Mellon University
ECE Department
Homework 2 – 18-421/623
Fall 2023

Instructions:	**Due Date(s):**
• 623 students: Exercises 1-2 are required. • 421 students: Exercises 1-2 are required. • For the Cadence design problems, 623 students and 421 students have different specifications.	• Wednesday, September 27, 2023 – 11:59PM EST **via Gradescope upload** • Extendible to Friday, September 29, 2023 – 11:59PM EST **via Gradescope upload***

Discussing the homework with other students is authorized but submissions must be individual
***This means you may turn in the homework up to that date with no penalty. Homework will not be accepted beyond this date.**

Exercise 1 (50 pts): Source Follower

In this exercise, we will use the GPDK 45 nm process to build a source follower (common drain) circuit shown in Fig. 1.1 The small signal voltage gain is measured as v_{out}/v_{in} in the small-signal domain, and similarly the output resistance v_{load}/i_{load} is measured by applying an ideal current source at the output with the input at AC ground.

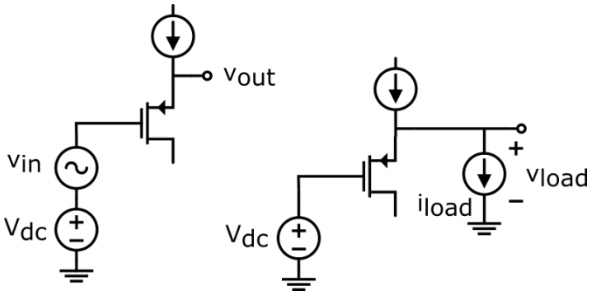


Fig 1.1 Voltage gain and output resistance

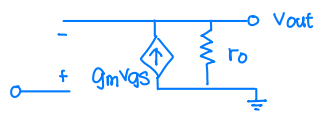
1) Draw a small-signal model for a source follower biased using ideal current sources.

2) Determine the small-signal gain of your ideal source follower (in terms of V_{GS}, V_{TH}, λ, and I_D)? Does I_D affect your small-signal gain?

3) Determine the output resistance of your ideal source follower (in terms of V_{GS}, V_{TH}, λ, and I_D)? Does W/L affect your output resistance with a constant V_{GS}-V_{TH}?

Exercise 1

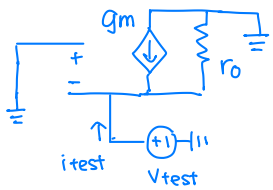
1)



2) $V_{out} = g_m (V_{in} - V_{out}) r_o \Rightarrow V_{out}/V_{in} = \frac{g_m r_o}{g_m r_o + 1}$, where $g_m = \frac{2I_D}{V_{SG}-V_{TH}}$, $r_o = \frac{1}{\lambda I_D} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{2}{\lambda(V_{SG}-V_{TH})+2}$

No. I_D doesn't affect the SS gain

3)



$V_{test} = (i_{test} + g_m(-v_{test}))\, r_o$

$\Rightarrow v_{test}(g_m r_o + 1) = i_{test} r_o \Rightarrow R_{out} = \frac{r_o}{g_m r_o + 1} = \frac{1}{g_m} // r_o = \frac{V_{SG}-V_{TH}}{I_D[\lambda(V_{SG}-V_{TH})+2]}$

$\approx \frac{1}{g_m} = \frac{V_{SG}-V_{TH}}{2I_D}$

4) Redraw a small-signal model for a source follower but biased this time using a non-ideal current source formed using current mirrors as shown in Fig. 1.2.

5) Determine the small-signal gain of your non-ideal source follower (in terms of V_{GS}, V_{TH}, λ, and I_D)? How does it compare to the ideal version?

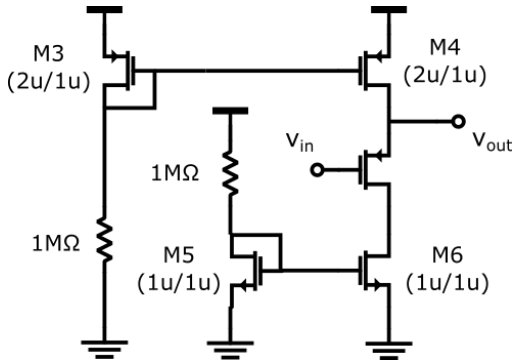
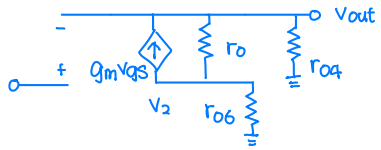


Fig 1.2 Source follower

4)



5) $\begin{cases} \frac{V_{out}}{r_{o4}} + \frac{V_{out}-V_2}{r_o} = g_m(V_{in}-V_{out}) \\ g_m(V_{in}-V_{out}) + (V_2-V_{out})/r_o + V_2/r_{o6} = 0 \end{cases}$

① + ② ⇒ $V_{out}/r_{o4} = -V_2/r_{o6} \Rightarrow V_2 = -V_{out} \times \frac{r_{o6}}{r_{o4}}$

① ⇒ $g_m V_{in} = g_m V_{out} + \frac{V_{out}}{r_{o4}} + \frac{V_{out}}{r_o} + V_{out}/(r_o r_{o4}/r_{o6}) \Rightarrow A_v = g_m/(g_m + \frac{1}{r_{o4}} + \frac{1}{r_o} + \frac{1}{r_o r_{o4}/r_{o6}})$

Since $r_o = r_{o4} = r_{o6} = 1/\lambda I_D \Rightarrow A_v = g_m/(g_m + 3\lambda I_D) = \frac{2}{3\lambda V_{ov}+2} = \frac{1}{1+1.5\lambda V_{ov}}$

Since $r_o = r_{o4} = 1/\lambda_p I_D$, $r_{o6} = 1/\lambda_n I_D$, $g_m = 2I_D/V_{ov}$

$A_v = 2/(2+\lambda_p V_{ov} + \lambda_p V_{ov} \times (\lambda_p/\lambda_n)) = \frac{1}{1+\lambda_p(1+\frac{\lambda_p}{2\lambda_n})V_{ov}}$

6) What is the output resistance of your non-ideal source follower (in terms of V_{GS}, V_{TH}, λ, and I_D)?

6) $\begin{cases} \frac{V_{load}}{r_{o4}} + \frac{V_{load}-V_2}{r_o} = g_m(0-V_{load}) + i_{load} \\ g_m(0-V_{load}) + \frac{V_2-V_{load}}{r_o} + \frac{V_2}{r_{o6}} = 0 \end{cases}$

② ⇒ $V_2(\frac{1}{r_o}+\frac{1}{r_{o6}}) = V_{load}(g_m+\frac{1}{r_o}) \Rightarrow V_2 = V_{load} \times \frac{g_m + 1/r_o}{1/r_o + 1/r_{o6}}$

① ⇒ $1/r_{out} = i_{load}/V_{load} = \frac{1}{r_{o4}} + \frac{1}{r_o} - \frac{1}{r_o} \times \frac{g_m+1/r_o}{1/r_o+1/r_{o6}} + g_m$

Since $r_o = r_{o4} = r_{o6} = 1/\lambda I_D$, $g_m = 2I_D/V_{ov}$

$\Rightarrow r_{out} = r_{o4} /\!/ r_o /\!/ -r_o(\frac{1}{\lambda V_{ov}}+\frac{1}{2})^{-1} /\!/ \frac{1}{g_m} = \frac{1}{\lambda I_D + \lambda I_D - \lambda I_D \times (\frac{1}{2}+\frac{1}{\lambda V_{ov}}) + \frac{2I_D}{V_{ov}}} = \frac{V_{ov}}{I_D(1+1.5\lambda V_{ov})} \approx V_{ov}/I_D$

(#2) Since $r_o = r_{o4} = r_{o6}$ and $g_m \gg 1/r_o$

$\Rightarrow 1/r_{out} \approx \frac{1}{r_{o4}} + \frac{1}{r_o} - \frac{1}{2}g_m + g_m = \lambda I_D + \lambda I_D + \frac{1}{2} \times 2I_D/V_{ov} \Rightarrow r_{out} = \frac{V_{ov}}{I_D(1+2\lambda V_{ov})}$

(#3) $r_o = r_{o4} = 1/\lambda_p I_D$, $r_{o6} = 1/\lambda_n I_D$, $g_m = 2I_D/V_{ov}$

$\Rightarrow 1/r_{out} = \lambda_p I_D + \lambda_p I_D - \lambda_p I_D \times \frac{2/\lambda_p V_{ov}+1}{1+\lambda_n/\lambda_p} + 2I_D/V_{ov} = (I_D/V_{ov})(2\lambda_p V_{ov} - \lambda_p V_{ov} \times \frac{2/\lambda_p V_{ov}+1}{1+\lambda_n/\lambda_p} +)$

$= (I_D/V_{ov})(2+2\lambda_p V_{ov} - \frac{2+\lambda_p V_{ov}}{1+\lambda_n/\lambda_p}) = (I_D/V_{ov})(\frac{2\lambda_n}{\lambda_p+\lambda_n} + \lambda_p V_{ov}(2-\frac{\lambda_p}{\lambda_p+\lambda_n}))$

$\Rightarrow r_{out} = (V_{ov}/I_D)[\frac{2\lambda_n}{\lambda_p+\lambda_n} + \lambda_p V_{ov}(2-\frac{\lambda_p}{\lambda_p+\lambda_n})]^{-1}$

7) CADENCE: Design and simulate a source follower[1] using GPDK 45 nm process using the circuit shown in Fig. 2. Size the transistor M_1 to achieve a voltage gain of Av > .8 V/V (18-623 students) or of (18-421: 0.75) and an output resistance ranging from 60 to 80 kΩ (18-623) or in the range of 50 to 100 kΩ (18–421). Use V_{DD} = 1V. Submit your design in netlist format (starting with "subckt source_follower GND IN OUT VDD" and ending with "ends source_follower").

8) What's the operation region for each transistor in your design

7,8) Since large W/L gives you small $V_{SG}-V_{TH}$, and increases your gain

Using M_1 with size 100u/1u and V_{IN} = 650mV gives you A_v = 0.81 and r_{out} = 73.4 kΩ

[1] For the transistors, use "nmos1v" and "pmos1v". And for the resistors, you can use "res" from analogLib

Exercise 2 (50 pts): Super Source Follower

In this exercise, we will use the GPDK 45nm process to implement a super source follower (Fig. 2.1). A super source follower uses a common-source amplifier in a feedback mode at the output stage of a source follower STA to reduce its output resistance.

1) Using ideal current sources, draw the small-signal model of the super-source follower.

2) What is the small-signal gain of the ideal super source follower? How does it compare to the ideal from Exercise 5 (assume the transistors are all the same size)?

3) What is the output resistance of the ideal super source follower? How does it compare to the ideal from Exercise 5 (assume the transistors are all the same size, and $g_{m1}=g_{m2}$, $r_{O1}=r_{O2}$)?

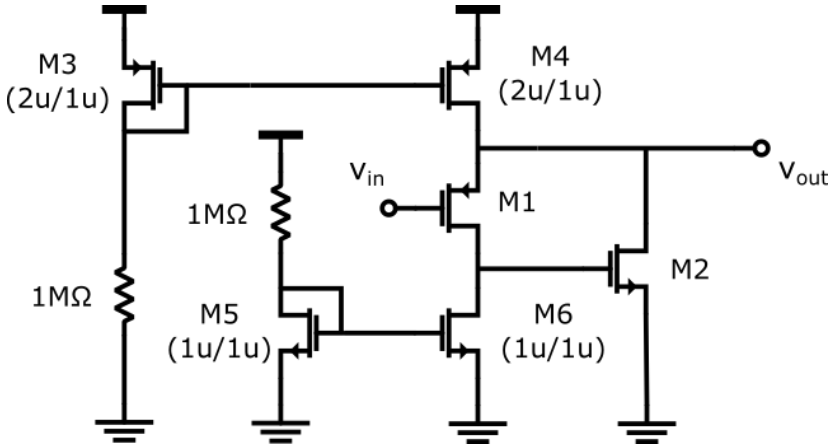


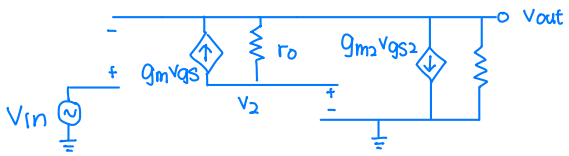
Fig 2.1 Super source follower schematic

2)

$$\begin{cases} g_m(V_{in}-V_{out}) = (V_{out}-V_2)/r_O + V_{out}/r_{O2} + g_{m2}V_2 \\ g_m(V_{in}-V_{out}) + (V_2-V_{out})/r_O = 0 \end{cases}$$

① − ② ⇒ $V_{out}/r_{O2} + g_{m2}V_2 = 0$

⇒ $V_2 = -V_{out}/g_{m2}r_{O2}$



Substitute into ①

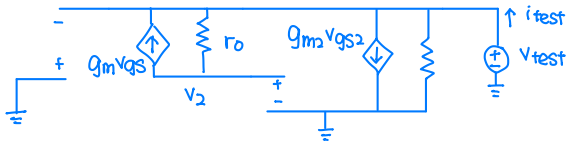
⇒ $g_m V_{in} = g_m V_{out} + V_{out}/r_O + V_{out}/g_{m2}r_{O2}r_O$

⇒ $V_{out}/V_{in} = g_m/(g_m + \frac{1}{r_O} + \frac{1}{g_{m2}r_{O2}r_O}) = \frac{g_m r_O}{g_m r_O + 1 + 1/g_{m2}r_{O2}}$ < $Gain_{SF} = \frac{g_m r_O}{g_m r_O + 1}$

3)

$$\begin{cases} i_{test} + g_m(0-V_{test}) + \frac{V_2-V_{test}}{r_O} = g_{m2}V_2 + \frac{V_{test}}{r_{O2}} \\ g_m(0-V_{test}) + (V_2-V_{test})/r_O = 0 \end{cases}$$

② ⇒ $V_2/r_O = V_{test}(g_m + 1/r_O)$ ⇒ $V_2 = V_{test}(g_m r_O + 1)$



Substitute into ①

⇒ $i_{test} = g_{m2}V_{test}(g_m r_O + 1) + V_{test}/r_{O2}$

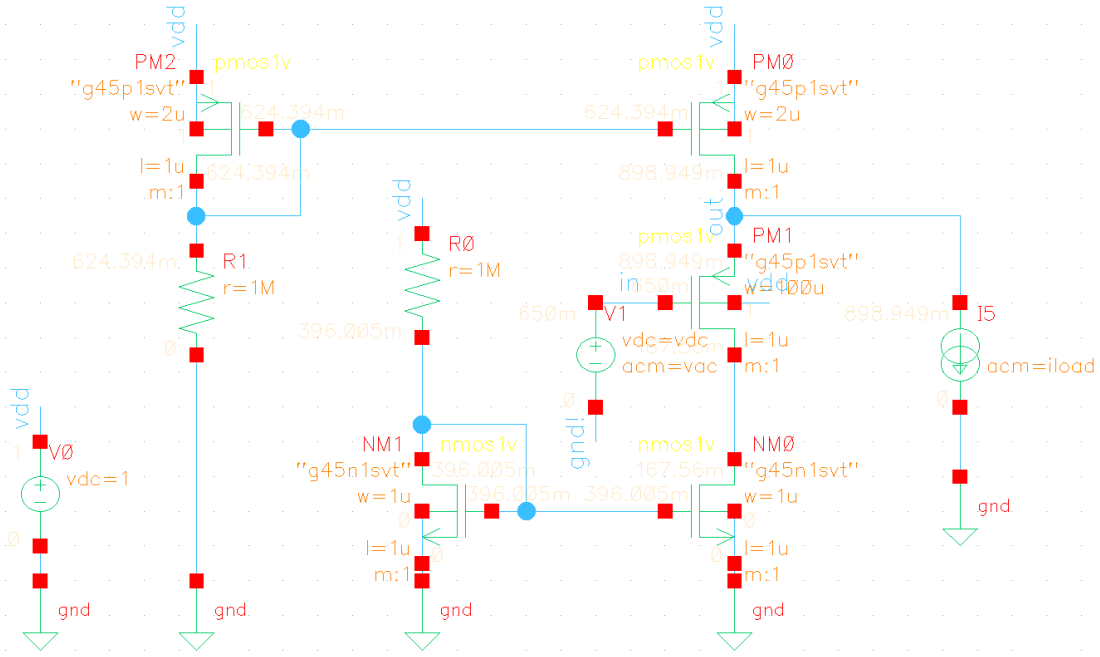
⇒ $i_{test} = V_{test}[g_{m2}(g_m r_O + 1) + \frac{1}{r_{O2}}]$ ⇒ $R_{out} = r_{O2} /\!/ \frac{1}{g_{m2}} /\!/ \frac{1}{g_{m2}(g_m r_O)} \approx \frac{1}{g_{m2}(g_m r_O)}$ < $r_{out,SF} = \frac{1}{g_m} /\!/ r_{O1}$

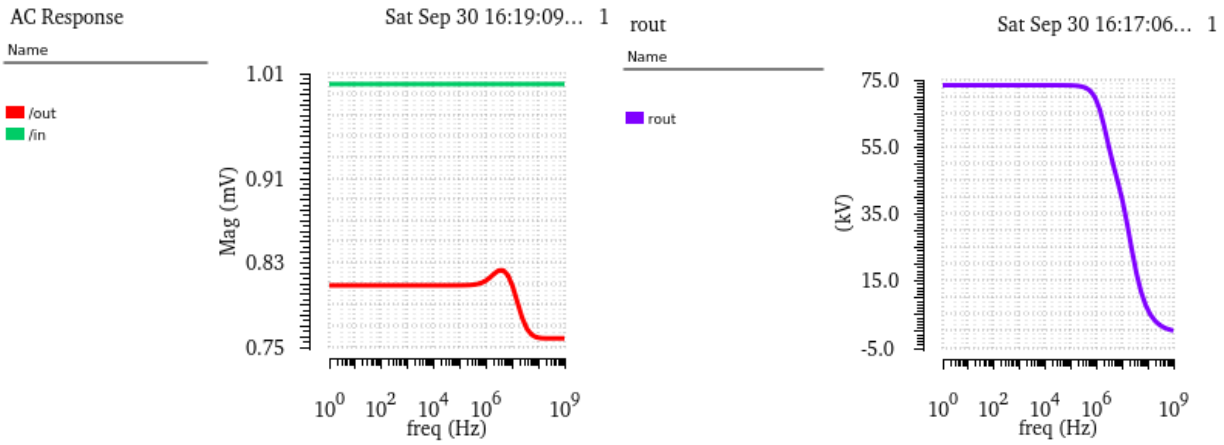
4) Build and simulate the super source follower and size transistor M2 to achieve an output resistance < 30 kΩ (18-623) or < 50 kΩ (18-421). Use V_{DD} = 1V. Submit your design in netlist format (starting with "subckt super_source_follower GND IN OUT VDD" and ending with "ends super_source_follower.")

The following design parameter achieves 15.3 kΩ output resistance and A_V = 0.885 in low frequency

M_1	M_2	V_{IN}
100u / 1u	1u / 1u	200mV

Results from source follower simulation (Gain = 0.81, r_{out} = 73.4k)





Results from SSF simulation (Gain = 0.885, r_{out} = 15.3k)

