Carnegie Mellon University
ECE Department
Homework 1 – 18-421/623
Fall 2023

Instructions:	**Due Date(s):**
• 623 students: Exercises 1& 2 are required. • 421 students: Exercise 1 is required, Exercise 2 is optional and counts for extra credit	• Friday, 9-8-2023 – 11:59PM EST **via Canvas upload** • Extendible to Monday, 9-11-2023 – 11:59PM EST **via Canvas upload***

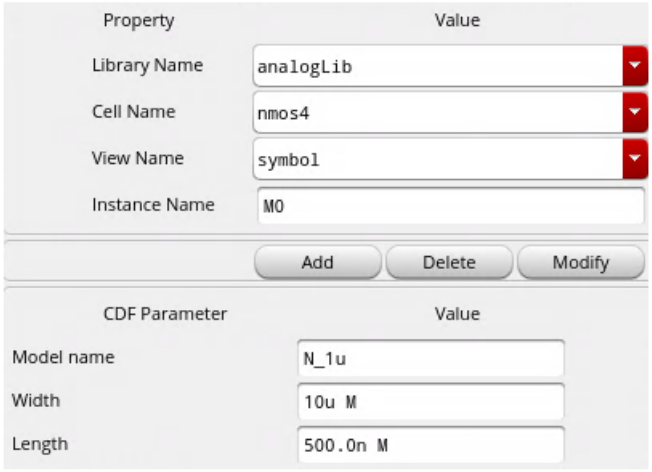
Discussing the homework with other students is <u>authorized</u> but submissions must be individual
*** This means you may turn in the homework up to that date with no penalty. Homework will not be accepted beyond this date.**

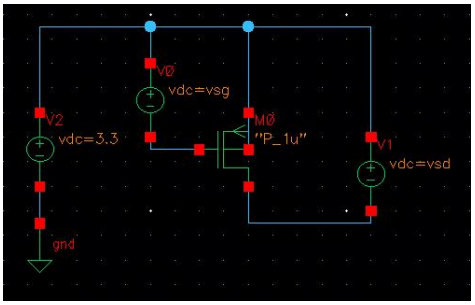
Exercise 1 (40pts): Simulating Circuits with Virtuoso

For this homework assignment, you have to use Cadence Virtuoso. Your submission must include

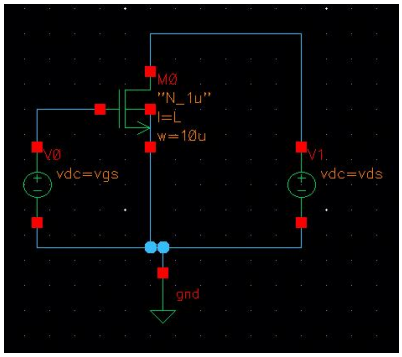
i) The schematic drawings (**screenshots from Cadence** with legible labels/texts)
ii) Plots with **white background** and **thick line widths**
iii) **Short comments** on the plots/results

In this homework, we will use the **long channel transistors** given in the model file */afs/ece/class/ece623/F22/cmosedu_models*. The figure on the right gives an example of how to place an instance of the NMOS to use from the **analogLib** library. We will use **nmos4** cell which will follow the **N_1u** model from the model card.





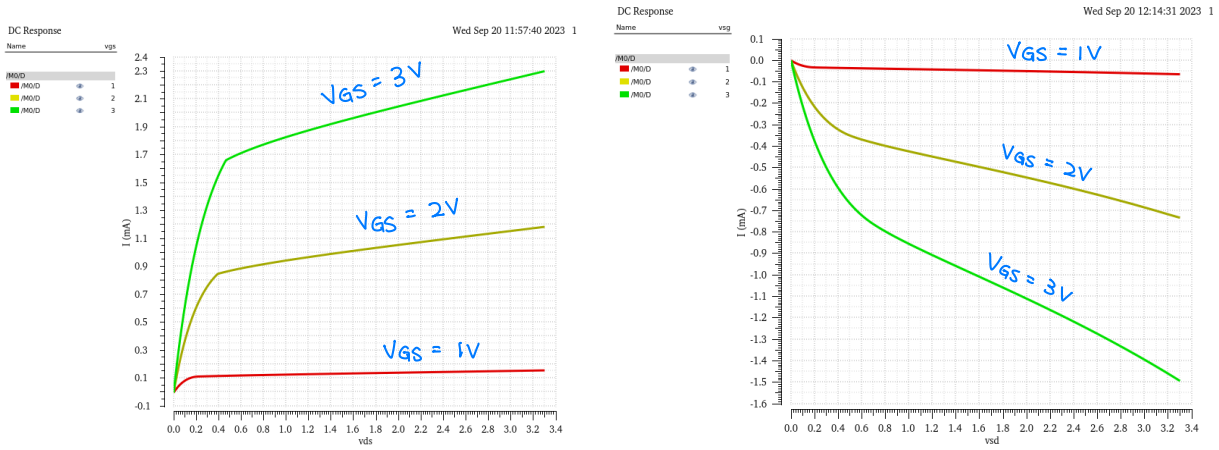
Schematic to characterize a PMOS



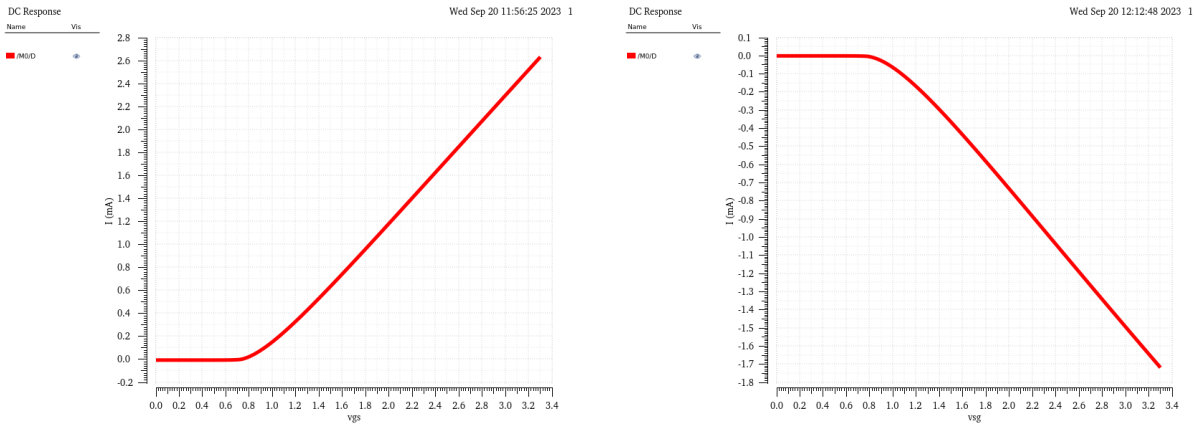
Schematic to characterize an NMOS

Change the appropriate fields when you instantiate the PMOS transistor (**pnmos4, P_1u**).

1) Perform an I_D vs. V_{DS} (or V_{SD}) sweep for both NMOS and PMOS devices for at least 3 different values of V_{GS} (V_{SG}). Set L = 0.5u and W = 10u, for each device. **(3 pts)**



2) Perform an I_D vs. V_{GS} (V_{SG}) sweep for both NMOS and PMOS devices. Assume that V_{DS} extends the full power supply range (e.g., from V_{DD} to ground, pick V_{DD} = 3.3V). **(3 pts)**



3) Using your curves in 1) and 2), estimate the following:
   a. The resistance of the devices in the **triode region** for at least three cases **(4 pts)**
   b. The resistance of the devices in the **saturation region** for at least three cases **(4 pts)**
   c. The lambda parameter of the devices for at least three cases **(4 pts)**
   d. The threshold voltage of each device **(4 pts)**

a. When V_{gs} = 1V / 2V / 3V, an NMOS transistor has a resistance 1120 / 262 / 159 Ω (estimated in V_{ds} = 50mV)
When V_{sg} = 1V / 2V / 3V, an PMOS transistor has a resistance 3760 / 763 / 454 Ω

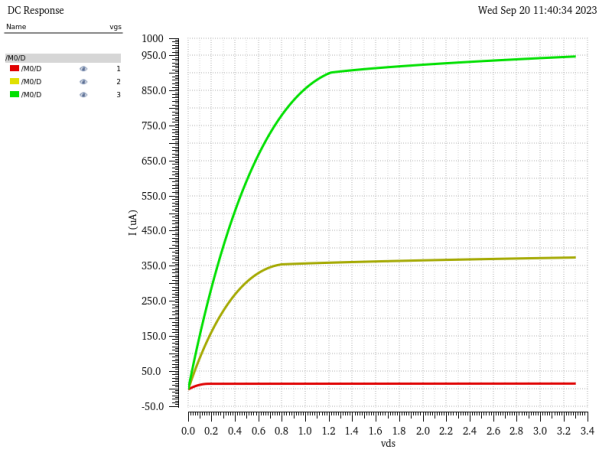
b. When V_{gs} = 1V / 2V / 3V, an NMOS transistor has a resistance 79.8 / 10.1 / 5.2 kΩ (estimated in V_{ds} = 3V)
When V_{sg} = 1V / 2V / 3V, an PMOS transistor has a resistance 84.1 / 6.64 / 3.2 kΩ

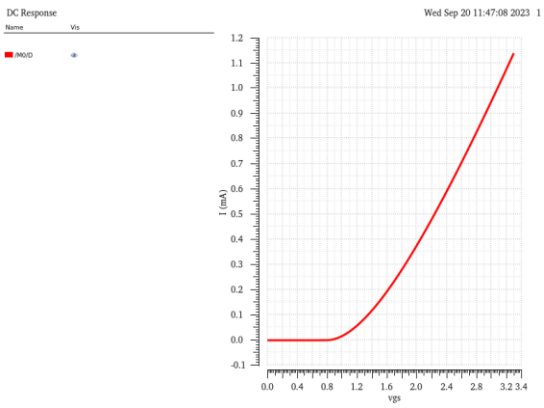
C. When V_{gs} = 1V / 2V / 3V, an NMOS transistor has a lambda 0.081 / 0.085 / 0.081 (estimated in V_{ds} = 3V)
When V_{sg} = 1V / 2V / 3V, an PMOS transistor has a lambda 0.200 / 0.226 / 0.228

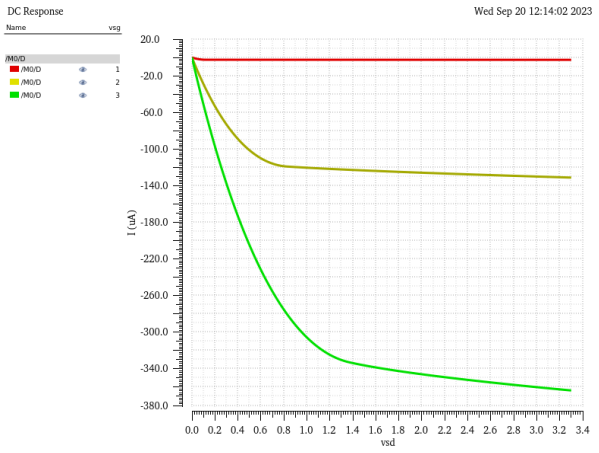
d. NMOS : 868 mV, PMOS : -950 mV

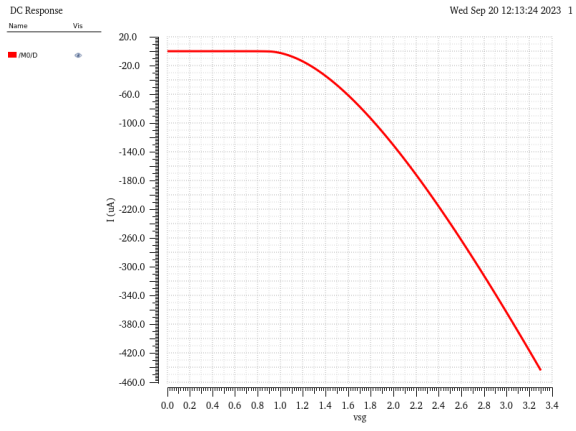
4) Estimate these values (a-d. above) when **L = 1.5u and W = 10u,** for each device and for the same corresponding biases you used in part 3. **Present them in a table with the results from 3) for comparison.** **(12 pts)**

5) Discuss the differences between 3) and 4) if any with possible reasons behind them. **(6 pts)**









4)

		Rtriode (Ω)	Rsat (kΩ)	lambda	V_{TH}
L = 0.5μ	NMOS	1120 / 262 / 159	198 / 10.1 / 5.2	0.081 / 0.085 / 0.081	0.87
	PMOS	3760 / 763 / 454	84.1 / 6.64 / 3.2	0.200 / 0.226 / 0.228	0.86
L = 1.5μ	NMOS	7100 / 1080 / 631	5900 / 168 / 59.9	0.010 / 0.015 / 0.017	1.0
	PMOS	36200 / 3390 / 1930	30.8k / 257 / 79.7	0.013 / 0.294 / 0.341	1.1

5) Longer-channel transistors have larger resistance and smaller lambda due to less short-channel effect. PMOS has a higher resistance in triode region

Exercise 2 (20pts): Process Parameter Estimation from Simulation

Assume that you know the transistor's aspect ratio, and further assume that the foundry has provided you with a model for simulating this transistor but that you cannot view the contents of the model card. We want to derive some simulation parameters: **the process transconductance** ($k = \mu_n C_{OX}$), **the threshold voltage (V_{TH})**, and the short-channel parameter (λ), from our simulation results.

Hint: Building up for Cadence GPDK 45nm process is in Cadence lab 1

1) Write down the equation set you want to evaluate the process (e.g. square law model)
2) Describe your method to derive **the process transconductance** ($k = \mu_n C_{OX}$) from your simulation.
3) Describe your method to derive **the threshold voltage** (V_{TH}) from your simulation.
4) Describe your method to derive **the short-channel parameter** (λ) from your simulation.
5) Evaluate Cadence GPDK 45nm process and finish the table below for NMOS and PMOS

Length (μm)	Width (μm)	PMOS			NMOS		
		$\mu_n C_{OX}$ (μA/V)	V_{TH} (V)	λ (V^{-1})	$\mu_n C_{OX}$ (μA/V)	V_{TH} (V)	λ (V^{-1})
2.0	20.0	215	.305	.121	353	.382	.105
	10.0	214	.304	.121	353	.381	.104
	5.0	213	.302	.120	352	.378	.103
1.0	20.0	212	.322	.148	342	.404	.138
	10.0	212	.322	.148	343	.403	.138
	5.0	212	.321	.147	343	.400	.136
	2.0	209	.318	.146	341	.393	.135
0.5	10.0	230	.348	.185	303	.433	.189
	5.0	230	.348	.186	304	.432	.188
	2.0	228	.348	.187	305	.429	.187
	1.0	225	.346	.185	306	.422	.184
0.2	10.0	211	.405	.266	252	.490	.299
	5.0	210	.405	.267	254	.489	.297
	2.0	209	.405	.268	258	.486	.292
	1.0	207	.403	.265	262	.480	.285
	0.5	204	.400	.259	267	.470	.279

Exercise 2

General: $L = 2.0\,\mu m$ and $L = 1.0\,\mu m$ are implemented with finger = 2
$L = 0.5\,\mu m$ and $L = 0.2\,\mu m$ are implemented with finger = 1

Vth: V_{gs}, V_{ds} should not affect V_{TH} too much (<5%)
The values are obtained from $V_{gs} = 0.5V$, $V_{ds} = 0.1V$
Multi-finger transistors make threshold lower a little bit (<10mV)

λ: λ is estimated by $\lambda = g_{ds} / I_D$ in saturation region
The values are obtained from $V_{gs} = 0.6V$, $V_{ds} = 0.8V$
λ has a large variance with V_{ds} ($V_{ds} = 0.5V$: 1.5x, $V_{ds} = 1V$: 0.8x)
V_{gs} ($V_{gs} = 0.5V$: 1.2x, $V_{gs} = 0.8V$: 0.9x)
Multi-finger transistors doesn't make a large difference

$\mu_n C_{ox}$: $\mu_n C_{ox}$ is estimated by $I_D / [(W/L) V_{DS} (V_{GS} - V_{TH} - \frac{1}{2} V_{DS})]$ in triode region (This assumes $\lambda(V_{DS} - V_{DSAT}) \ll 1$)
The values are obtained from $V_{gs} = 0.8V$, $V_{ds} = 0.1V$
$\mu_n C_{ox}$ has a small variance with V_{ds} (<3%) and V_{gs} (<10%)
Multi-finger transistors make a lower $\mu_n C_{ox}$ ($\sim 20\,\mu A/V^2$)
$\mu_n C_{ox}$ in PMOS has lower value due to (1) smaller I_D (2) smaller V_{TH}