# DP1 Recitation #2

Ching-Yi Lin

# Outline

- Announcements
- Discussion
  - Testbench introduction
  - Current mirrors
  - Voltage biasing
- OH (~6:00)

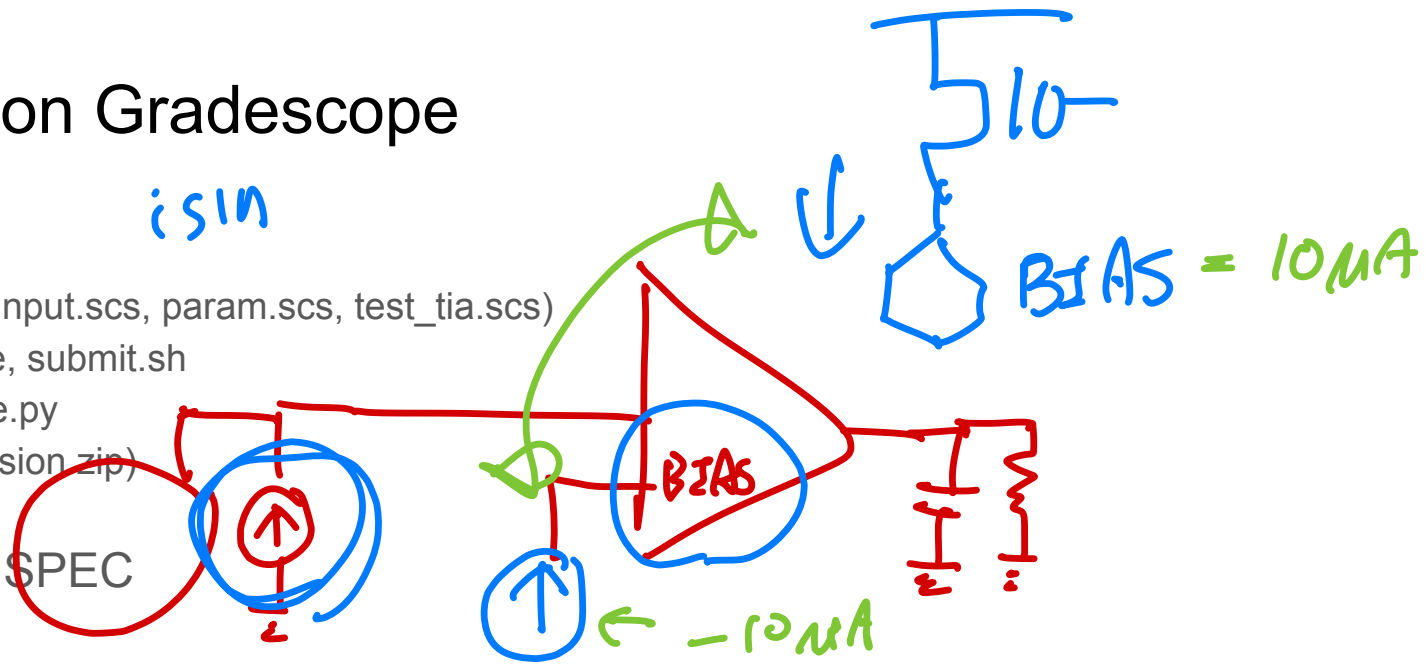
# Announcements

1. DP1 hand analysis score is on Canvas
    a. Full score (20/20) if you are not late

2. DP1 report template is on Canvas

# Testbench on Gradescope

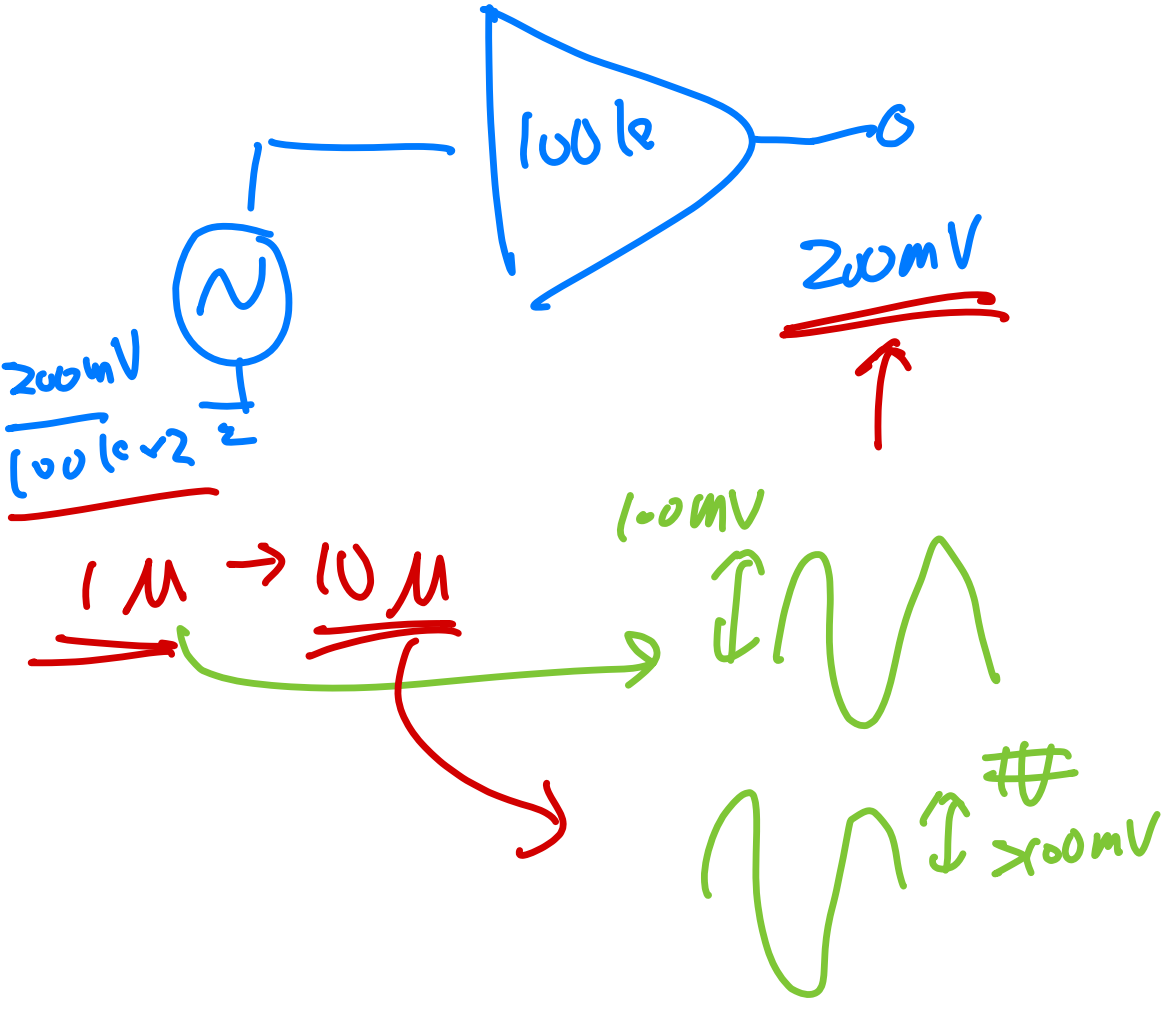
- Files
  - Netlist (input.scs, param.scs, test_tia.scs)
  - Makefile, submit.sh
  - evaluate.py
  - (submission.zip)
- Testbench SPEC



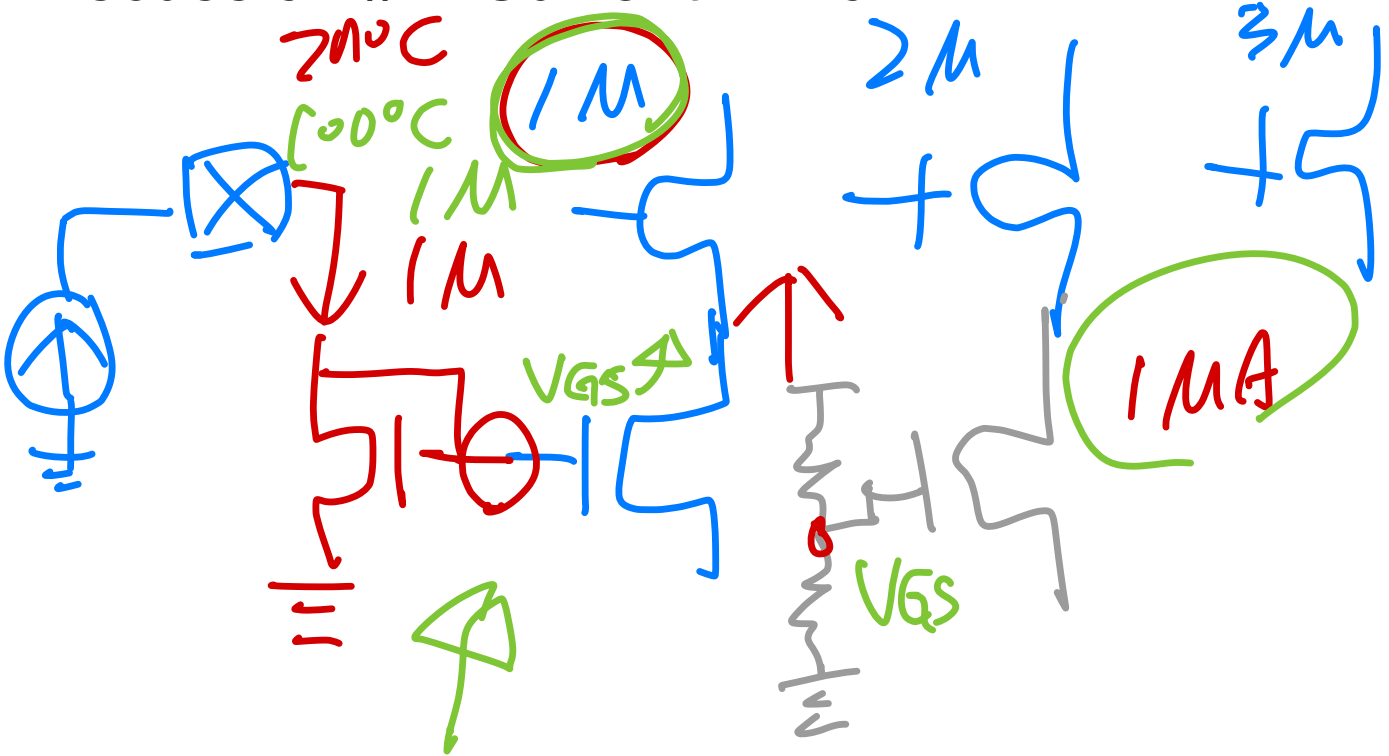

- Autograder only evaluates on 27C, but your report needs 0C, 27C, and 100C

```
chingyil@ece-gui-000:/afs/ece/class/ece623/F23/DP1/submission_template$ ls
evaluate.py  input.scs  Makefile  param.scs  README.md  spectre.dc  spectre.fc  spectre.ic  submit.sh  test_tia.scs
```

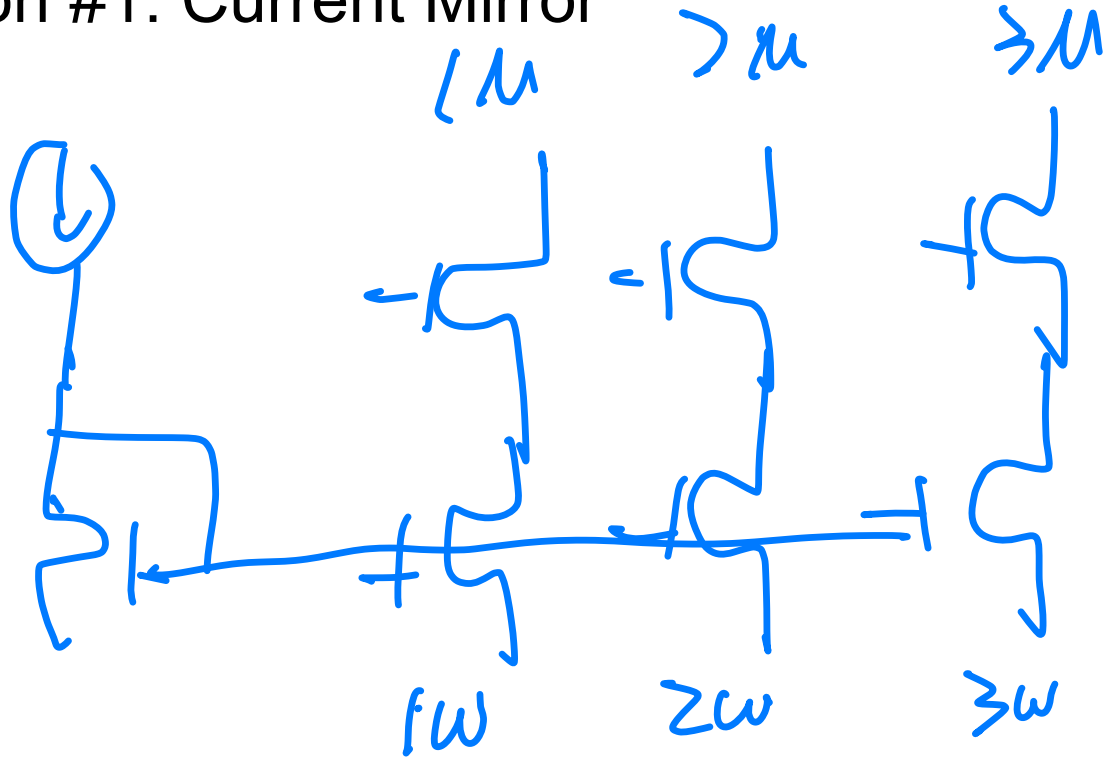
# Output swing



# Discussion #1: Current Mirror



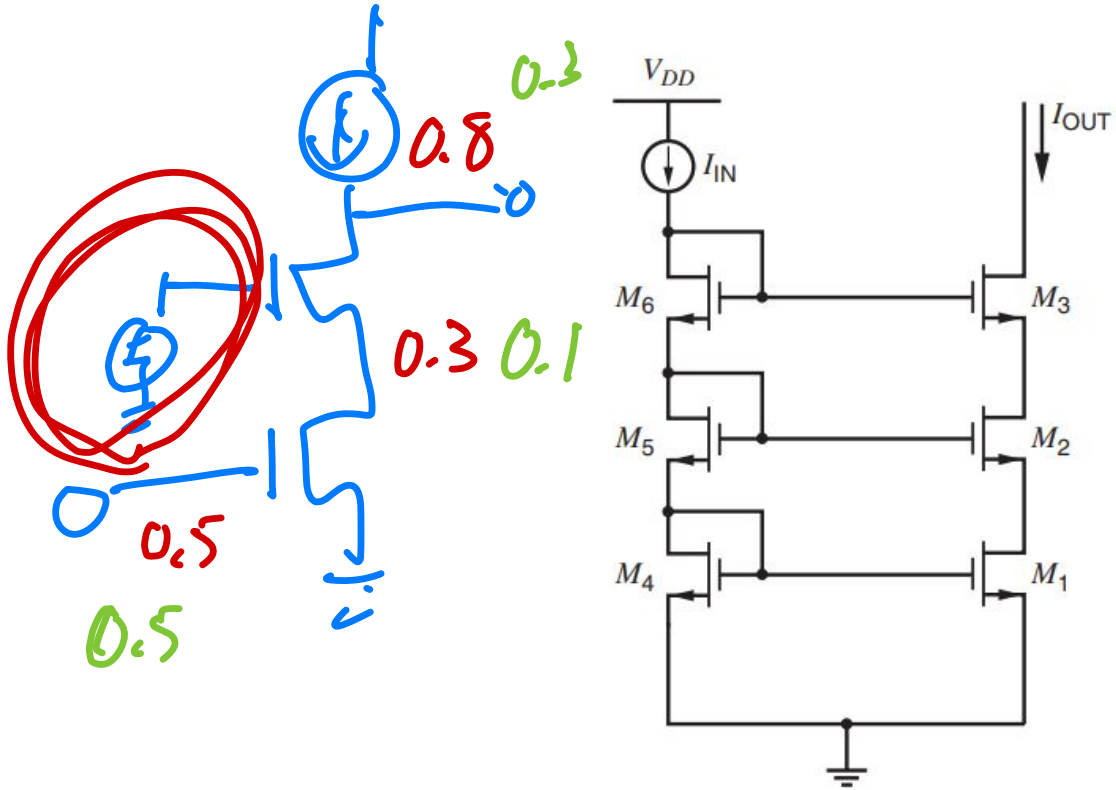
# Discussion #1: Current Mirror



# Discussion #2: Voltage Biasing

Options

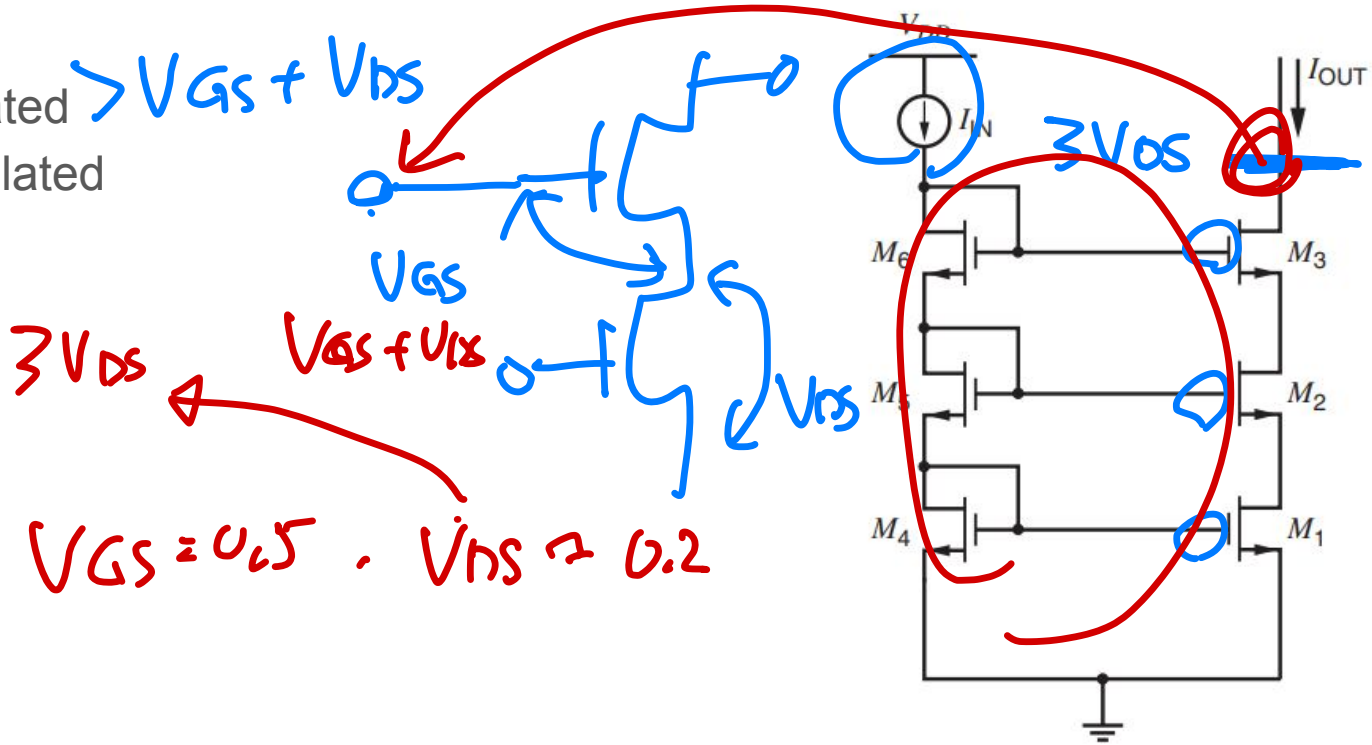
- Resistor-related
- Transistor-related



# Discussion #2: Voltage Biasing

Options

- Resistor-related
- Transistor-related



# Discussion #2: Voltage Biasing

# Office Hour (~6:00)

- No schematic debug, such as
  - Why my gain / Rin / bandwidth is lower than I expected
  - Why my Vout is at this level

- No KVL, KCL, algebra check